

WHAT IS CLAIMED IS:

1. A method for manufacturing a ferroelectric capacitor,

2 comprising:

3 forming a first electrode layer;

4 forming a ferroelectric dielectric layer over the first  
5 electrode layer;

6 planarizing the ferroelectric dielectric layer to form a  
7 planarized ferroelectric dielectric layer; and

8 forming a second electrode layer over the planarized  
9 ferroelectric dielectric layer.

2. The method as recited in Claim 1 wherein planarizing the

2 ferroelectric dielectric layer includes planarizing the  
3 ferroelectric dielectric layer using a chemical mechanical  
4 polishing process until it is substantially planar.

3. The method as recited in Claim 2 wherein the

2 substantially planar ferroelectric dielectric layer has an average  
3 surface roughness of less than about 1 nm.

4. The method as recited in Claim 3 wherein the

2 substantially planar ferroelectric dielectric layer has an average  
3 surface roughness of less than about 0.5 nm.

5. The method as recited in Claim 1 wherein the  
2 ferroelectric dielectric layer comprises lead zirconate titanate  
3 (PZT) or strontium bismuth tantalate (SBT).

6. The method as recited in Claim 1 further including  
2 cleaning the planarized ferroelectric dielectric layer prior to  
3 forming the second electrode layer.

7. The method as recited in Claim 1 further including  
2 forming a first protective layer between the first electrode layer  
3 and a conductive plug and forming a second protective layer over  
4 the second electrode layer.

8. The method as recited in Claim 7 further including  
2 planarizing at least a portion of the second electrode layer to  
3 form a planarized second electrode layer prior to forming the  
4 second protective layer.

9. The method as recited in Claim 8 further including  
2 cleaning the planarized second electrode layer prior to forming the  
3 second protective layer.

10. The method as recited in Claim 1 further including  
2 planarizing at least a portion of the first electrode layer to form

3       a planarized first electrode layer prior to forming the  
4       ferroelectric dielectric layer.

11. The method as recited in Claim 10 further including  
2       cleaning the planarized first electrode layer prior to forming the  
3       ferroelectric dielectric layer.

12. The method as recited in Claim 1 wherein the  
2       ferroelectric dielectric layer has a thickness ranging from about  
3       150 nm to about 60 nm and the planarized ferroelectric dielectric  
4       layer has a thickness ranging from about 100 nm to about 20 nm.

13. The method as recited in Claim 1 further including  
2       patterning the first electrode layer, the ferroelectric dielectric  
3       layer, and the second electrode layer to form a patterned  
4       ferroelectric capacitor.

14. A ferroelectric capacitor, comprising:

2           a first electrode layer;

3           a substantially planar ferroelectric dielectric layer located  
4       over the first electrode layer, wherein the substantially planar  
5       ferroelectric dielectric layer has an average surface roughness of  
6       less than about 4 nm; and

7           a second electrode layer located over the substantially planar  
8       ferroelectric dielectric layer.

15. The ferroelectric capacitor as recited in Claim 14

2       wherein the substantially planar ferroelectric dielectric layer has  
3       an average surface roughness of less than about 1 nm.

16. The ferroelectric capacitor as recited in Claim 14

2       wherein the substantially planar ferroelectric dielectric layer  
3       comprises lead zirconate titanate (PZT) or strontium bismuth  
4       tantalate (SBT).

17. A method for manufacturing a ferroelectric random access

2 memory (FeRAM) device, comprising:

3 forming a transistor having source/drain regions over a

4 semiconductor substrate;

5 forming an interlevel dielectric layer over the transistor,

6 the interlevel dielectric layer having a conductive plug therein

7 contacting at least one of the source/drain regions; and

8 forming a ferroelectric capacitor over the interlevel

9 dielectric layer and contacting the conductive plug, including;

10 forming a first electrode layer over the conductive plug;

11 forming a ferroelectric dielectric layer over the first

12 electrode layer;

13 planarizing the ferroelectric dielectric layer to form a

14 planarized ferroelectric dielectric layer; and

15 forming a second electrode layer over the planarized

16 ferroelectric dielectric layer.

18. The method as recited in Claim 17 wherein planarizing the

2 ferroelectric dielectric layer includes planarizing the

3 ferroelectric dielectric layer using a chemical mechanical

4 polishing process until it is substantially planar.

19. The method as recited in Claim 18 wherein the

2 substantially planar ferroelectric dielectric layer has an average

3 surface roughness of less than about 1 nm.

20. The method as recited in Claim 19 wherein the  
2 substantially planar ferroelectric dielectric layer has an average  
3 surface roughness of less than about 0.5 nm.

21. The method as recited in Claim 17 wherein the  
2 ferroelectric dielectric layer comprises lead zirconate titanate  
3 (PZT) or strontium bismuth tantalate (SBT).

22. The method as recited in Claim 17 further including  
2 cleaning the planarized ferroelectric dielectric layer prior to  
3 forming the second electrode layer.

23. The method as recited in Claim 17 further including  
2 forming a first protective layer between the first electrode layer  
3 and a conductive plug and forming a second protective layer over  
4 the second electrode layer.

24. The method as recited in Claim 23 further including  
2 planarizing at least a portion of the second electrode layer to  
3 form a planarized second electrode layer prior to forming the  
4 second protective layer.

25. The method as recited in Claim 24 further including  
2       cleaning the planarized second electrode layer prior to forming the  
3       second protective layer.

26. The method as recited in Claim 17 further including  
2       planarizing at least a portion of the first electrode layer to form  
3       a planarized first electrode layer prior to forming the  
4       ferroelectric dielectric layer.

27. The method as recited in Claim 26 further including  
2       cleaning the planarized first electrode layer prior to forming the  
3       ferroelectric dielectric layer.

28. The method as recited in Claim 17 wherein the  
2       ferroelectric dielectric layer has a thickness ranging from about  
3       150 nm to about 60 nm and the planarized ferroelectric dielectric  
4       layer has a thickness ranging from about 100 nm to about 20 nm.

29. The method as recited in Claim 17 further including  
2       patterning the first electrode layer, the ferroelectric dielectric  
3       layer, and the second electrode layer to form a patterned  
ferroelectric capacitor.

30. A method for manufacturing a ferroelectric capacitor,

2 comprising:

3 forming a first electrode layer;

4 forming a ferroelectric dielectric layer over the first  
5 electrode layer; and

6 forming a second electrode layer over the planarized  
7 ferroelectric dielectric layer, wherein at least one of the first  
8 electrode layer, ferroelectric dielectric layer or second electrode  
9 layer is planarizing to form a planarized first electrode layer,  
10 planarized ferroelectric dielectric layer or planarized second  
11 electrode layer, respectively.

31. The method as recited in Claim 30 wherein the

2 ferroelectric dielectric layer is planarized and cleaned prior to  
3 forming the second electrode layer.

32. The method as recited in Claim 30 wherein the second

2 electrode layer is planarized and cleaned prior to forming an  
3 additional layer thereon.